REMARKS

Claims 93 and 95-101 were pending prior to entry of these amendments. Claims 97-99 are withdrawn. Claims 93, 95, 96, 100, and 101 are amended herein. New Claim 102 is added.

Rejections Under 35 U.S.C. §102

Claims 93, 95, 96, 100, and 101 are rejected under 35 U.S.C. §102(e) as being anticipated by Mayer et al., U.S. Patent No. 6,315,883. Independent Claim 93, has been amended to recite a method of forming a planar conductive structure usable in manufacturing an interconnect for an integrated circuit, the method comprising providing a substrate having a top portion that includes a surface portion and a cavity portion, wherein the cavity portion has at least a first cavity having a width of less than one micron and a second cavity having a width larger than 10 microns; and depositing a planar conductive layer within the cavity portion and on the surface portion, wherein the planar conductive layer, as deposited, has a predetermined thickness range over the surface portion that is between one tenth and one half of the thickness of the planar conductive layer within the cavity portion. Dependent Claims 95, 96, 100, and 101 have been amended to conform to the amendment to Claim 93. These amendments are fully supported by the specification as originally filed.

The pending claims have been amended to recite a ***method***, rather than a structure. Mayer et al. do not disclose or suggest a ***method*** of depositing a planar conductive layer within the cavity portion and on the surface portion, wherein the planar conductive layer, as deposited, has a predetermined thickness range over the surface portion that is between one tenth and one half of the thickness of the planar conductive layer within the cavity portion" (emphasis added).

The Examiner contends that "the product claimed by applicant is considered to be anticipated or at least obvious over the product depicted in the figure on the front of the Mayer et al. patent" (Figure 7). Applicants respectfully submit that Figure 7 of Mayer et al. shows an end product ***after an electropolishing step*** (*see* Mayer et al., Col. 9, line 54 – Col. 10, line, 11. The structure shown in Figure 7 of Mayer et al. is not obtained by depositing (as claimed), but by ***planarization by electropolishing*** a separately deposited conductive layer 211. The deposited conductive layer 211 of the Mayer et al. process is shown in Figure 3. Applicants respectfully submit that the structure shown in Figure 3 of Mayer et al. does not have a deposited ***planar***

conductive layer. As shown in Figure 3 of Mayer et al, the conductive layer 211 recesses or "nips" 215 as well as recesses 213. Thus, Mayer et al. do not disclose or suggest ***a method of depositing*** a planar conductor layer within the cavity portion and on the surface portion, wherein the planar conductive layer, as deposited, has a predetermined thickness range over the surface portion that is between one tenth and one half of the thickness of the planar conductive layer within the cavity portion, as recited in amended Claim 93.

Claim 93, as amended, is therefore patentable as it is not anticipated by Mayer et al. Claims 95, 96, 100, and 101, as amended, which depend from and include all of the limitations of amended Claim 93, are therefore also patentable. Furthermore, each of the dependent claims recites further distinguishing features of particular utility.

Rejections Under 35 U.S.C. §103

Claims 93, 95, 96, 100, and 101 are rejected under 35 U.S.C. §103(a) as being unpatentable over Mayer et al. As discussed above, Mayer et al. do not teach or suggest ***a method of depositing*** a planar conductor layer within the cavity portion and on the surface portion, wherein the planar conductive layer, as deposited, has a predetermined thickness range over the surface portion that is between one tenth and one half of the thickness of the planar conductive layer within the cavity portion, as recited in amended Claim 93. Applicants respectfully submit that Mayer et al. actually teach away from a ***method of depositing a planar*** conductive layer within the cavity portion and on the surface portion, wherein the planar conductive layer, as deposited, has a predetermined thickness range over the surface portion that is between one tenth and one half of the thickness of the planar conductive layer within the cavity portion, as recited in amended Claim 93. As noted above, Mayer et al. teach to electropolish in order to ***planarize*** filled surface of features ***after*** the conductive layer is deposited. Mayer et al. do not teach or suggest ***depositing a planar conductive layer*** within the cavity portion and on the surface portion, as recited in Claim 93, as amended.

Therefore, Claim 93, as amended, is patentable as it is not obvious in view of Mayer et al. Claims 95, 96, 100, and 101, as amended, which depend from and include all of the limitations of amended Claim 93, are also patentable. Furthermore, each of the dependent claims recites further distinguishing features of particular utility.

New Claim

New Claim 102 is added and is fully supported by the specification, as originally filed at, for example, page 11, lines 5-21.

Conclusion

Applicants respectfully submit that all of the pending claims are patentably distinguishable over the prior art of record. The cited references, either alone or in combination, do not teach or suggest Applicants' claimed invention.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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AMEND

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